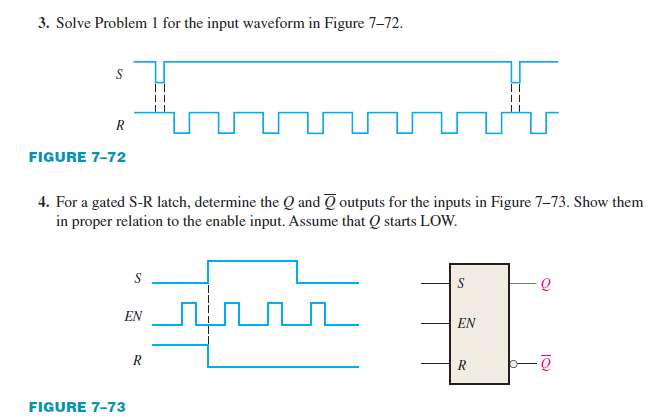
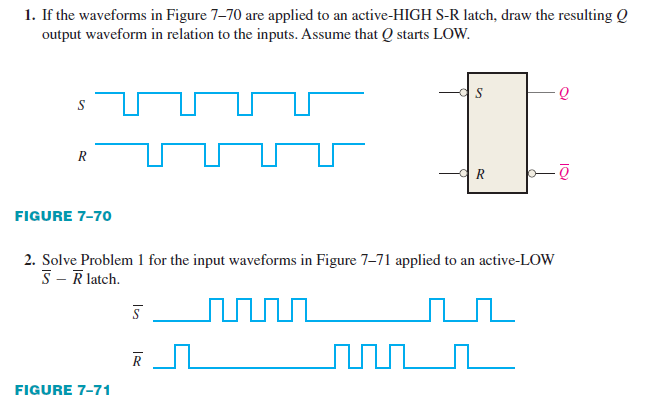
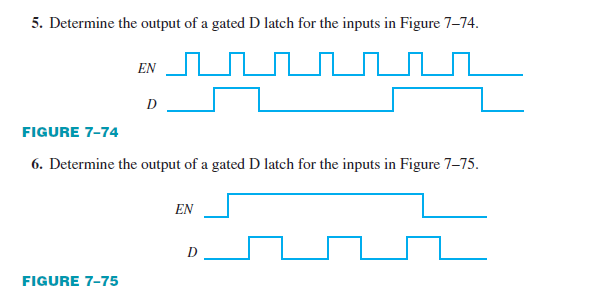
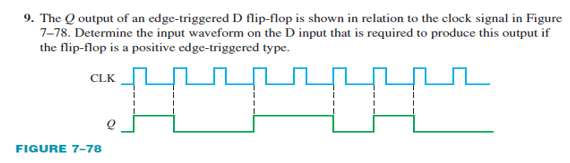
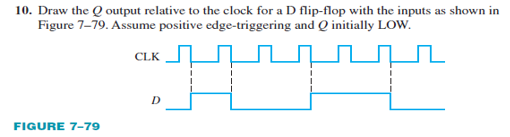
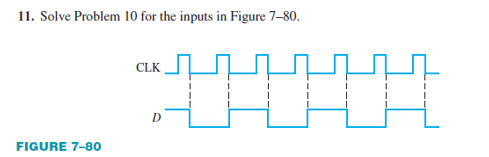
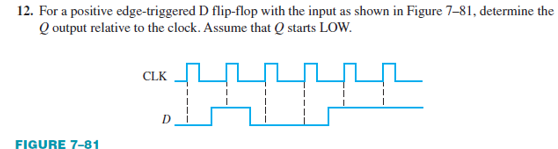
**Assignment-4**

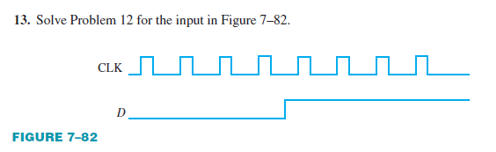


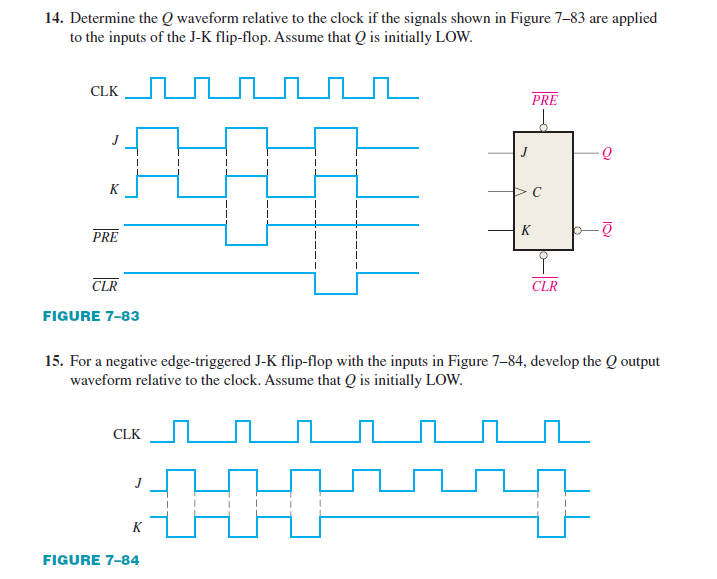


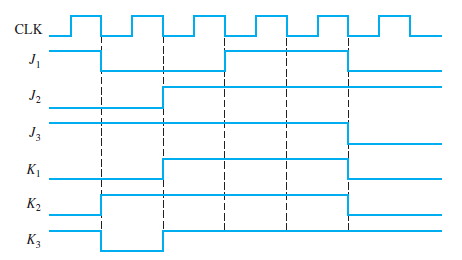




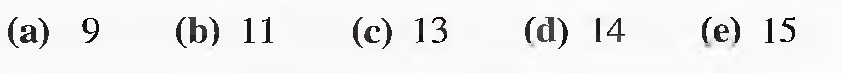




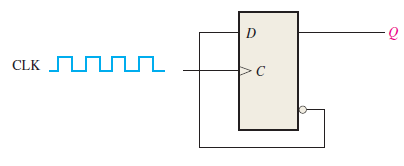
1. For the circuit in Figure -1, complete the timing diagram in Figure 2 by showing the Q output (which is initially LOW). Assume PRE and CLR remain HIGH.



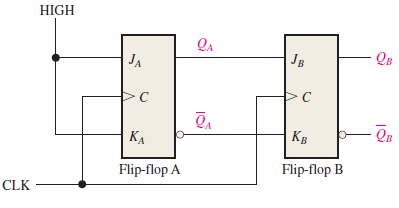
1. Show how to connect a 4-bit asynchronous counter for each of the following moduli. Also for 30kHz clock determine the frequency at the output of each counter.



1. A D flip-flop is connected as shown in Figure 7–90. Determine the Q output in relation to the clock. What specific function does this device perform?



1. For the circuit in Figure, develop a timing diagram for eight clock pulses, showing the QA and QB outputs in relation to the clock.



22. Design a counter to produce the following binary sequence. Use J-K flip-flops.

1, 4, 3, 5, 7, 6, 2, 1, ….

23. Design a counter to produce the following binary sequence. Use J-K flip-flops.

0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, …

24. Design a binary counter with the sequence shown in the state diagram of Figure. (using D flip flop)

